THE FRONT-END BOARD FOR THE ATLAS LIQUID ARGON CALORIMETER.

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ABSTRACT

The very high collision rate and the scarcity of interesting events foreseen at the future Large Hadron Collider at CERN require the development of new types of readout electronics structures. Among those, the dual port analog memories provide the possibility to decrease the high rates of incoming data. These memories allow indeed to perform the analog to digital conversion only after the level 1 trigger, thus dividing by at least a factor 100 the amount of samples to digitise, and to use much slower ADCs. Nevertheless, this induces that they are able to sample the incoming analog signal at high frequency (40 MHz for the LHC) and to store it waiting for the level 1 trigger latency. Moreover, the very high dynamic range of the detector signal requires the analog memory to cover at least 12 bits of resolution, even with a multigain system.

The Laboratoire de l'Accélérateur Linéaire (LAL) from Orsay, the Nevis Laboratories from Irvington, the University of Alberta from Edmonton and the CEA-DAPNIA from Saclay have developed a complete readout solution to fit the requirements of the ATLAS liquid argon calorimeter system. The upstream part of the chain consists in warm preamps followed by tri-gain bipolar shapers, dual port analog memories (also named " analog pipelines " or " Switch Capacitor Arrays "), and 12bit-5MHz ADCs. All these components are gathered on a large board, which provides the readout of 128 calorimeter channels. The first prototypes of the board give entire satisfaction.

1. REQUIREMENTS

The basic requirements for the readout system are the following :

- Amplify and shape the signal coming from the detector with an optimisation of the signal to both electronics and pile-up noise ratios.
- Sample at 40 MHz the signals coming out of the shapers.
- Store data during the level 1 trigger latency (>= 2us).
- Read several samples (typically 5) per event accepted by level 1 (the maximum rate should be 75 kHz and could raise up to 100 kHz) and perform the analog to digital conversion.
- Format and transmit the data to remote DSP boards ("R.O.D") which will provide on the fly feature and energy extractions before sending data to the level 2 event buffers.
- Operate fully simultaneous write and read operations and deal with interleaved events.
- Cover a dynamic range of 16 bits without degrading the calorimeter resolution (0.7% for the largest signals).
- Feed the level 1 trigger system with analog sums of the input signals.

The total number of channels to be equipped is very high (~200,000) and the electronics has to fit in a limited volume with stringent constraints on power dissipation and accessibility. Furthermore, the radiation level to deal with is at the level of 100 krad per year, including a safety margin of a factor 5.

2. SYSTEM DESIGN

The front-end electronics of the liquid argon calorimeter is located directly on the detector. There are around 60 crates, which house four different types of boards (see Fig. 1).

The idea to design a 128-channel readout board arose at the end of 1996. To match the above requirements, the following solutions were chosen (see Fig. 2) :

- The signal shape is bipolar with a rise time of 40ns to optimise pile-up versus electronics noise.
- The detector signals dynamic range of 16 bits outgoing the preamplifiers is divided in three linear ranges of 12 bits. This operation, performed by tri-gain shapers (gains of 1, 10, 100), allows to split the dynamic range without degrading the intrinsic detector resolution (~7 bits).
- Each signal coming out of the shapers is send to analog memories. Inside each memory, the signal is sampled at 40 MHz and stored until a level 1 trigger is received.
- Then only the interesting data is converted by the ADC (1% of the total input rate) with all samples on the same gain and sent serially to the output drivers.

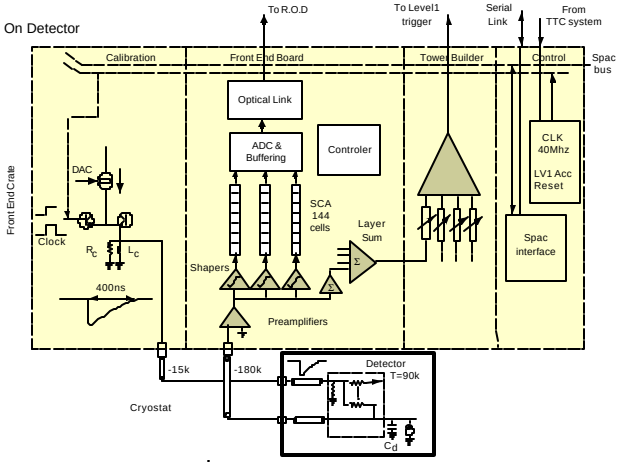

Fig. 1 : overview of the front-end electronics

The main difficulty to deal with was of course the digital to analog potential crosstalk. To check the validity of the chosen solution, a 16-channel prototype of the board was first designed. It included the front-end part of the board up to the ADC and the data formatters. The excellent results obtained proved the feasibility of the solution and gave encouragement to go on with the whole 128 channel board.

3. *FRONT-END BOARD* SPECIFICATIONS

This board treats the 128 channels coming from the detector in 16 groups of 8 channels (see Fig.2). Each block includes :

- two 4-channel preamps [1].
- two 4-channel tri-gain shapers [2].
- two 4x3-channel analog memories or SCA (Switched Capacitor Arrays).
- one 12bit / 5MHz ADC.

There is also a large amount of digital components to ensure all the functionnalities :

- 8 Altera FPGAs for gain selection and output data formatting (each for 16 channels).
- 2 Xilinx SCA controllers (each for 64 channels) which provide write and read addresses to the SCA and perform the synchronisation for all the read operations [9].
- A summation block for the first step of level 1 trigger analog sums.
- The TTC interface for the fast signals (CLK, L1, INIT).
- The interface for the new fast serial link (SPAC) which allows the downloading of all electronics sited on the detector.

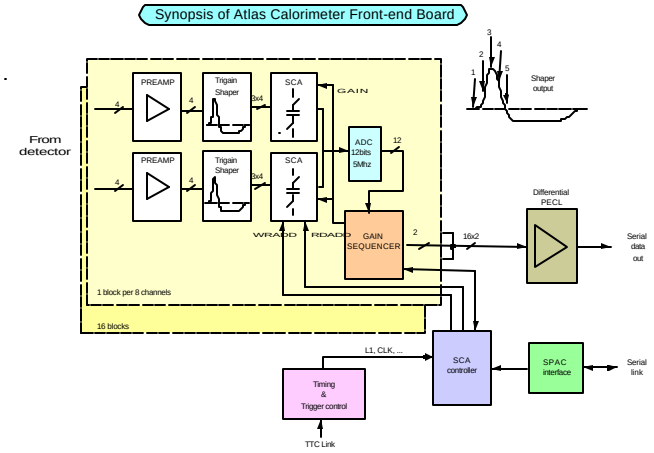

Fig. 2 : block diagram of the *Front-end board*

The signals coming out of the shapers are sent to the analog memories. Inside each memory, the signals are sampled at 40 MHz and stored until the SCA controller receives a level 1 trigger. Then the five samples corresponding to the selected event will be driven sequentially towards the output of the chips. At this point and for each sample, the 2x4 internal channels of two associated chips are multiplexed at a 5 MHz rate.

For each channel, the peak sample (the third sample) is first read. It is compared on the medium gain both to saturation and to a low threshold. Depending on the result of the comparison, one of the gains is chosen and stored. Then the same sample is read once again on the right gain, and sent to the output. All the four other samples are also read on the same gain as the peak sample. The total time needed for reading a group of 8 channels with 5 samples is thus 9us.

Event output data is formatted in a block of 50 16bit-words and sent serially on two lines (one for each byte) towards the R.O.D boards [10].

On the *Front-end board*, special care has been taken to avoid as much as possible the crosstalk between the digital part running either at 40 or at 5 MHz and the analog signals. This implied the use of common ground planes covering the complete board, special routing of critical signals, and strong decoupling and filtering of power supplies. All the perturbative digital lines are transmitted in differential PECL. Moreover, all the critical analog elements are treated in a pseudo differential manner.

4. ANALOG MEMORY SPECIFICATIONS

During the ten past years, several teams ([3], [4], [5]) have developed high dynamic range analog memories for level 1 buffering in calorimetry applications. All these chips have weak and strong points. All of them can deal with dynamic range on the order of 12 bits, but need a power supply of 6V inadvisable for a high reliability of 1.2um or less CMOS technologies. In the chips without input analog buffers, an external resistor is needed in series in both the signal and return path, to avoid damping due to sampling switching. These extra resistors are undesirable and are responsible for crosstalk between channels via the common signal return path. The chip described in [5] also suffers from analog crosstalks, but only due to small layout imperfections.

Two teams (Nevis and Orsay/Saclay) have then combined their experience and efforts to design new circuits fitting exactly the requirements.

In this experiment, the electronics will have to withstand a total ionising dose higher than 100krad. The last chip, dedicated to the final application, uses the DMILL CMOS 0.8um rad-hard technology [7].

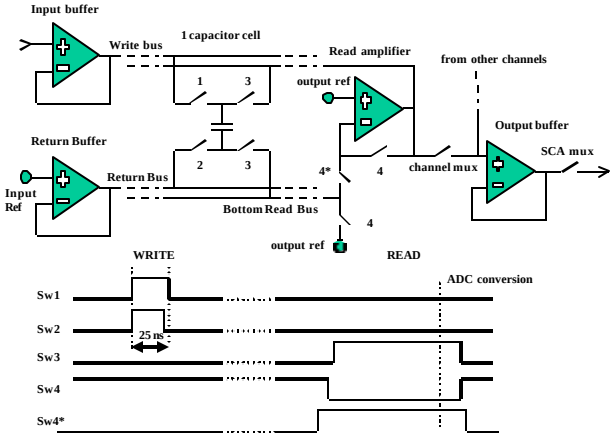

Fig. 3 : SCA channel architecture and sequences

The connection between the shaper and the pipeline is a critical point of the system. Consequently, in order to keep this connection short and to simplify the board layout, the two chips have the same modularity and use the same PQFP100 package.

Each gain of the four calorimeter channels treated by a shaper is stored in a pipeline channel. A 'slave' channel is associated with each group of three gains corresponding to a calorimeter channel. The input of this slave channel is connected to the reference output of the shaper. Its output is subtracted externally during read to the selected gain channel output. This pseudo-differential operation reduces drastically the coherent part of the noise induced within and in front of the pipeline. Unlike in [5], each slave channel corresponds to a different calorimeter cell. To limit a potentially catastrophic coupling from high gain to low gain, the channels are arranged as shown in Fig. 4.

Each of the 16 SCA channels consists in :

- 144 storage cells in which the signal is sampled at 40Mhz
- a write amplifier
- a return path amplifier
- a read-out amplifier.

The noise, the switching charge injection dispersion and the sensitivity to digital perturbation scale at first

order as 1/Cs. Thus a high value (1pF) has been chosen for the storage capacitor. The timings of the read, reset, and write operations, optimised for linearity, dynamic range and sampling time precision are shown in Fig. 3, and are described in detail in [5].

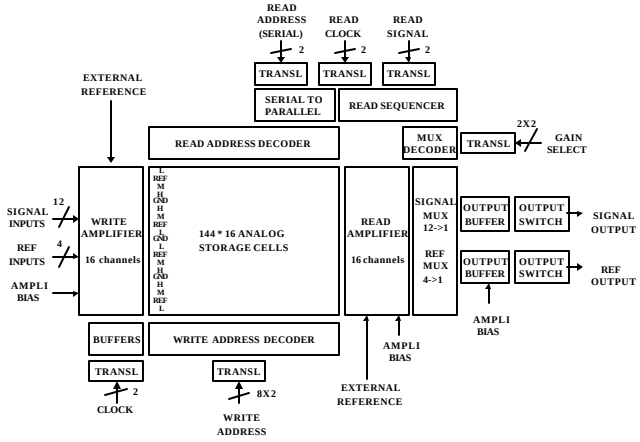

Fig. 4 : SCA layout architecture

Once a storage cell is read, the 4 groups are sequentially multiplexed at a 5Mhz rate toward two output buffers, one for the signal, the other for the reference. For each group, an external signal allows to select the proper gain. The output of the pipeline may be disabled using a switch. This allows multiplexing two SCAs toward a single ADC without extra electronics. All the amplifiers are described in [5] and have been optimised for high speed, low noise and rail to rail operation.

The digital part of the SCA has been designed to ensure the minimum digital activity. All the digital input signals are differential low level (LVDS or PECL). The write addresses, sent in parallel, are decoded using the power efficient scheme described in [4]. The read addresses are sent bit serially at the rate of the read clock before the read signal initiates the decoding of this address. Then the read-out and multiplexing operation is sequenced by the read clock. This sequence depends on a 'parity' static bit indicating whether the SCA is the first of the second one multiplexed toward the ADC.

	HP CHIP	HAMAC DMILL
POWER SUPPLIES	-1.7V/+3.3V	-1.7V/+3.3V
POWER CONSUMPTION	200mW	280mW(2)
MIN. DC SIGNAL (1)	-1V	-0.95V
MAX. DC SIGNAL (1)	2.8V	2.85V
Noise (uV rms)	270	300
Fixed Pattern Noise (uV rms)	120	190
DC Dynamic range	13.6 bits	13.3 bits
DC GAIN(2)	0.99	0.995
Cell to Cell DC GAIN dispersion	< 0.02% p-p	< 0.02% p-p
Channel Offset dispersion (rms)	10 mV	10mV
MAX. SHAPER SIGNAL	> 2.7V(*)	> 2.7V(*)
PEAK I.N.L. = (meas-fit) / max (3)	< +/- 0.1%(*)	< +/- 0.1%(*)
Sampling Jitter	< 45 ps rms*	< 45 ps rms *
Cell to Cell sampling time dispersion	266ps (p-p)	150ps (p-p)
Cell to Cell peak dispersion	0.07% p-p	0.05% p-p
DC channel-to-channel cross-talk	< 1^{E}-4 (*)	< 1^{E}-4 (*)
TRANSIENT ch-to-ch cross-talk	< 2.5^{E}-4	< 2.5^{E}-4
5Mhz Multiplexing residue	1^{E}-4	1^{E}-4
INPUT SLEW/RATE	120V/uS	175V/uS

Tab. 1 : performances of the SCA chips

(1) within +/- 0.5% integral nonlinearity

(2) reduction under study

(3) the transient characteristics have been measured using the signal delivered the medium gain of the integrated shaper [2] connected to a 0T amplifier with a detector capacitance of 680pF : signal range 0 to 2.5V.

(*) measurement limited by test setup.

A special care has been taken for the layout of this chip. Digital and analog parts have their private power supply lines and are clearly separated by guard rings. To avoid crosstalk, the distance between analog channels is intentionally kept large. The storage cells are as narrow as possible (26 um pitch) to minimise the write and bottom read bus parasitic capacitance. The write and return busses are large to lower their resistivity whereas the bottom read bus is very thin to lower the noise which is proportional to its capacitance [6].

The performances of both the HP and DMILL chips are summarised in Tab.1. They have both been characterised on the same dedicated test bench performing simultaneous write/read operation. All the present results have been measured with the chips mounted on sockets. Thus all are worst case and the values measured when mounted directly on the board are still better, especially for noise and crosstalk. The dynamic range is then close to 14 bits.

5. SPAC BUS SPECIFICATIONS

The aim of this protocol is to provide the loading and reading of all registers and memories located on the calorimeter of the ATLAS detector [8]. It has been designed to be fast (10Mbit/s), reliable (integrated error detection) and cheap. The slave interface fits in an unique circuit and offers several facilities (SPAC -> VME transcoder to drive a VME bus thus allowing crate interconnections, JTAG outputs for on board FPGA programming, ...). The SPAC bus can use PECL or BTL levels and be uni or bidirectionnal. User's software is written in C, and graphic interfaces are running on UNIX and MacIntosh. The SPAC bus induces small power consumption and is totally mute when not used. The protocol is simple and powerful, and allows an immediate understanding of data transfers with an oscilloscope.

SPAC general view

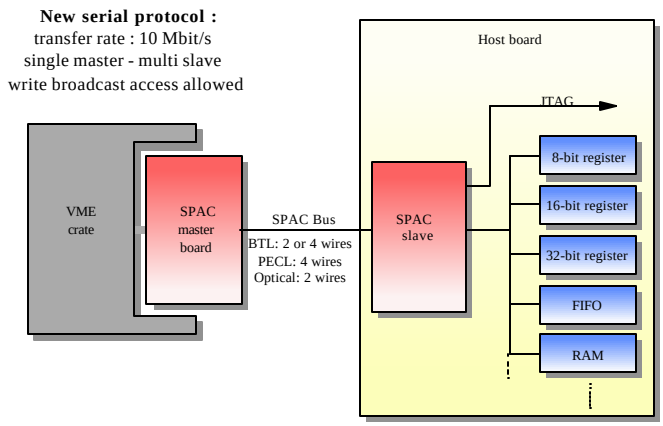

Fig. 5 : SPAC system architecture

Format of standard data transfers in the SPAC protocol

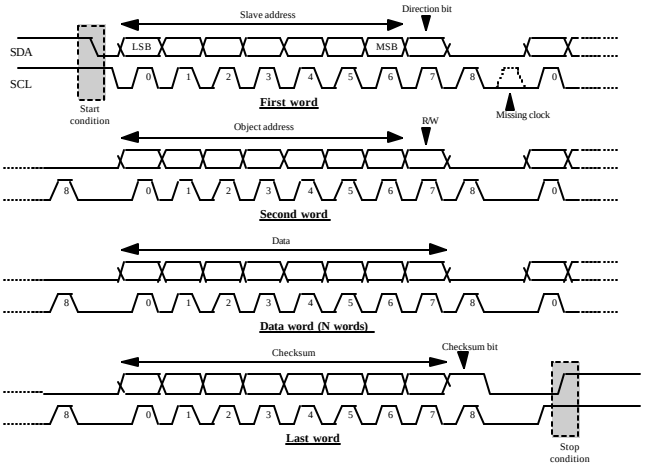

Fig. 6 : SPAC bit streams

The main points of this one-master n-slaves bus are described below (see Fig. 5). The following definitions allow any kind of transfer, including as many words as desired, in each direction between the master and the slaves. The specific adaptations for custom applications are left to the choice of the users.

Here follow the main features of the SPAC bus :

- The protocol requires only two bidirectionnal wires with BTL levels : SCL for clock/strobe, SDA for data (see Fig. 6). But it can be used identically with four unidirectional wires, in BTL or PECL technology. The master and slaves can either be considered as emitters or as receivers on the line.
- There is no problem of master arbitration as this bus is single-mastered by definition. Nevertheless, to prevent any collision, each emitter watches over the line before and while taking hand on it. Moreover, the protocol forbids the broadcast reading command.
- Each slave connected to the bus is addressable by a unique 7-bit address. One address is reserved for the global broadcast mode, which allows the addressing of all the slaves. Moreover, 15 other addresses are reserved for local broadcast modes, which allow the addressing of various groups of slaves, defined by the users. These groups realise a partition of the totality of the slaves (each slave belongs to one group). The broadcast modes are only available for write commands coming from the master.
- The data always travel in the same direction as the clock. Data is transferred at 10Mbit/s. The slaves use their local 40MHz clock to generate the 10MHz return data clock, so no additional clocks are needed. The slave interface clocks are internally resynchronised during each transfer from the master.
- The data packets are 9bit long (see below) with always exactly one missing clock period between packets. This allows to separate clearly the packets for simplicity purpose and gives time for data transfer within the receiver (this will help to simplify the receiver electronics). The 9bit words are transferred with LSB first (this allows the checksum to be calculated sequentially).
- The SDA and SCL lines follow the start and stop conditions of the I2C protocol. Conversely, there will be no acknowledging from the slave during a data transfer as this is the limiting point for the bus speed. In a general way, all the timings are secure as long as several conditions about the board distances are respected. This makes this system very safe.
- To prevent the collisions, the emitter always checks that the line is not busy before taking hand on it. Moreover the open collector structure protects the bus against any short.
- The format of the response to a read request is the same as the format of the request except for the direction bit in the first word. This means that the data contained in the two first words is a copy of the one received from the master. This allows crosscheck and makes the control software more convenient.
- The slave provides a JTAG output in order to program any other FPGA on the host board.
- There is a possibility for any slave to send an interruption to the master when the line is idle. This command has a special format (both lines pulled to zero during 10 clock cycles).

The SPAC is currently being used intensively and successfully in beam test at CERN. As its possibilities are wide, it may also be used for many other applications, as test benches in the lab. That is the case of the SCA test bench which provided all the previous results.

6. PERFORMANCES OF THE *FRONT-END BOARD*

Most of the original requirements have already been reached with the first 128-channel prototype. Five of these boards are currently used at CERN on test beam. The following results have their origin both in lab test benches and in beam tests.

- The total power dissipation is 96W per board, i-e 750mW per channel.
- The dynamic range is in excess of 18 bits without preamps. It is calculated by dividing the maximum output signal on the low gain (2500 ADC counts) by the noise in the high gain (0.8 ADC count). When connected to the detector, it goes down to 16 bits. The noise is indeed strongly depending on the cell capacitance and on the preamp input impedance (see Tab. 2).
- The integral nonlinearity stays below 0.2% over the full range with real signals (see Fig. 7).
- The noise distribution is gaussian. Its characteristics depend on the gain :
  - On the high gain, it is totally dominated by the preamp input, what is in respect with the requirements. The ratio between shaper and input noise is around 1/10 and between SCA and shaper around 1/2.5.
  - On the medium gain, it is still dominated by the input noise. The resolution is good (over 8 bits) as the noise amplitude is around 1 ADC count.
  - On the low gain, it is dominated by the last stages (shaper + SCA + ADC) but the value is nevertheless around 0.5 ADC count.

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Auteur:
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Aperçu:
Cette image EPS n'a pas été enregistrée
avec un aperçu intégré.
Commentaires:
Cette image EPS peut être imprimée sur une
imprimante PostScript mais pas sur
un autre type d'imprimante.

Fig. 7 : linearity with real signal on the *Front-End Board*

- The noise is distributed into two major contributions : incoherent and coherent. The latter can also be divided into two terms : one corresponding to groups of four channels that can be found everywhere on the board, and the other to the term common to all channels on the board. The major source of coherent noise is the pickup at the board input.

Noise/channel	Incoherent	Coherent/4	Coherent/board
High gain	3.5 to 7.8	1.3	1.2
Medium gain	1.2	0.2	0.3
Low gain	0. 6	0.03	0.3

Tab. 2 : noise results on the *Front-end board*
(in ADC counts -> 1 ADC count ~= 1mV)

- The sum over 128 channels is dominated by the noise contribution which is coherent per board in the high gain. This is therefore one of the main points to focus on. However, it appears currently not to be shared between two neighbouring boards, even without lateral shieldings.

7. CONCLUSION

Six 128 channel front-end boards have already been produced and tested in beam tests at CERN. The performances measured proved the validity of the technical choices. Most of the original requirements have already been reached. The main remaining difficulty is the coherent pickup at the board input. Thus the input connector shielding will be improved. Moreover, the current prototype is not radiation tolerant, what is a mandatory requirement at the level of 100krad for the production. However, some components as the analog memory designed in DMILL technology are already rad-hard and their performances could qualify them for the final run.

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